REMARKS

These remarks follow the order of the paragraphs of the office action. Relevant portions of the office action are shown indented and italicized.

DETAILED ACTION

1. Claims 8 and 16 are amended in response to the last office action. Claims 1-20 are presented for examination.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they are not corresponded with the following reference sign(s) mentioned in the description: reference numeral 1140 in fig 13 is pointing to POINTER rather than to FRAME as described frame descriptor 1140 in page 31, line 18 of the specification. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either ("Replacement Sheet" or "New Sheet pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action The objection to the drawings will not be held in abeyance.

In response, the applicants respectfully state that the drawing page 10 also marked 'replacement sheet' is amended and another set of drawings is included herewith.

Double Patenting

3. Claims 1-20 of this application conflict with claims 1-20 of Application No 10/619,988. 37 CFR 1.78(b) provides that when two or more applications filed by the same applicant contain conflicting claims, elimination of such claims from all but one application may be required fl the absence of good and sufficient reason for their retention during pendency n more than one application. Applicant is required to either cancel the conflicting claims from all but one application or maintain a clear line of demarcation between the applications See MPEP § 822.

In response, the applicants respectfully state that it is planned to file a terminal disclaimer for this application.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign county or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-20 are rejected under U.S.C. 102(b) as being anticipated by Osborne et al. [US 5,751,951].

In response, the applicant respectfully states that Claims 1 - 20 are apparently not anticipated by the invention of Osborne et al. The present invention, claimed in Claims 1 - 20:

"Methods, apparatus and systems are provided for controlling flow of data between a memory of a host computer system and a data communications interface for communicating data between the host computer system and a data communications network. In an example embodiment, apparatus comprises a descriptor table for storing a plurality of descriptors for access by the host computer system and data communications interface. Descriptor logic generates the descriptors for storage in the descriptor table. The descriptors include a branch descriptor comprising a link to another descriptor in the table."

Whereas, the cited art to Osborne et al , US Patent 5,751,951, filed: October 30, 1995, is entitled: "Network interface". The Osborne abstract reads:

"A packet based data transmission system includes a flexible optimized non-blocking transmit interface that incorporates optimized buffer modes, dynamic and static chaining, streaming and the utilization of small packet formats. Static chaining refers to connecting together the linked list for successive packets for the same transmit channel or virtual channel. Dynamic chaining refers to means by which the network interface performs this chaining automatically, thereby solving a blocking problem. On the transmit side, streaming refers to initiating the transmission of packet data before the entire packet data has been presented to the interface. This, in turn, permits more rapid recycling of the buffer space. On the receive side, streaming refers to initiating the processing of packet

> data before the entire packet has been received. The packet transmission system also includes a receive interface that incorporates a chunking system in which a buffer is divided into multiple chunks or segments to accommodate different size packets. Additionally, the receive interface includes an optimized linked list scheme to support chunking in which no linking element is required for the first buffer in the linked list. In one embodiment a small packet format is provided to reduce the relative overhead in sending small packets. In another embodiment the optimized buffer mode associated with the receive side can be utilized on the transmit interface for further reducing overhead."

*Thus Osborne is concerned with a "*non-blocking transmit interface that incorporates optimized buffer modes, dynamic and static chaining, streaming and the utilization of small packet formats.*" Osborne is not concerned with* a descriptor table, or apparatus for controlling flow of data between first and second data processing systems via a memory, *as in the present claims. Thus* Claims 1-20 are allowable under U.S.C. 102(b) as not being anticipated by Osborne.

> *As for claim 1, Osborne et al teach an apparatus comprising a descriptor table [e.g., ring queue 16 in fig. 2A], said apparatus for controlling flow of data between first and second data processing systems [fig. 3A] via a memory said descriptor table for storing a plurality of descriptors for access [col. 3, lines 28-42] by the first and second data processing systems- and descriptor logic for generating [e.g., col. 19, lines 46-47] the descriptors for storage In the descriptor table, the descriptors including a branch descriptor comprising a rink [e.g. fig. 2A] to another descriptor in the table.*

In response, the applicants respectfully state that exception is taken with the alleged equivalencies of the elements of claim 1 and Osborne. Claim 1 reads as follows:

> 1. An apparatus comprising: a descriptor table - said apparatus for controlling flow of data between first and second data processing systems via a memory, said descriptor table for storing a plurality of descriptors for access by the first and second data processing systems; and descriptor logic for generating the descriptors for storage in the descriptor table, the descriptors including a branch descriptor comprising a link to another descriptor in the table.

For example, apparently the "ring queue 16 in fig. 2A," of Osborne is not the "descriptor table" of claim 1. Ring queue 16 is a transmit input queue, not a descriptor table for storing descriptors. Osborne col. 9, lines 55-67 read as follows:

> Referring now to FIG. 1A, in the prior art on the transmit side a host memory 10 is coupled to the network via a network interface card or NIC 12 via an I/O bus 14. Ring queue 16 is a transmit input queue, called the TXin queue, containing as entries frame descriptors 22. Frame descriptor 22 points to a linked list of buffer descriptors 24 with buffers at 20 and 40 containing the data to be transmitted. After a frame of information has been transmitted, the frame is written into a transmit complete queue 18 called TXdone queue as a frame descriptor 26 which points to buffer descriptor or BD 24. This indicates to the host system that the frame descriptor and its associated buffer descriptors and buffers are no longer in use by the transmission mechanism.

Thus Ring queue 16 is a transmit input queue, not a descriptor table. The descriptor table in claim 1 is for storing a plurality of descriptors for access by the host computer system and data communications interface. This is apparently not the function of Osborne's 'ring queue 16' , which contains frame descriptors as entries.

Also, exception is taken with office communication statement above "*said apparatus for controlling flow of data between first and second data processing systems [fig. 3A]* ." Fig 3A apparently is not relevant to flow control between data processing systems. Fig 3A is described as:

> FIG. 3A is a block diagram showing an ATM network interface chip on a network interface card in which the subjects frame descriptors and buffer descriptors are used.

Osborne col. 14, lines 21-35 describes Fig. 3A as the following:

> Referring to FIG. 3A, in the subject invention the flexible format of frame descriptors and buffer descriptors permit the aforementioned functions and advantages. To illustrate how this is possible in general, an ATM network interface includes a network interface card 150 and a host computer 151. The frame descriptors and buffer descriptors are used for communication between host 151 and network interface card 150 over peripheral component interconnect or PCI bus 152. The communication includes control information for the ring queues and information describing the data to be transmitted or describing data received. This information belongs to the network interface. Though the ring queue containing frame descriptors and the buffer descriptors are commonly in host memory, they may also be in network interface local memory.

Thus Fig. 3A is not relevant to flow control between data processing systems.

Also, exception is taken with office communication statement above:

> "*via* a memory said descriptor table for storing a plurality of descriptors for access [col. 3, lines 28-42]"

Osborne *[col. 3, lines 28-42] reads:*

> "Small packets are particularly important for request-response styles of communication such as is common in client-server computing systems. It is therefore important that the design of the network interface accommodate small packets while at the same time being able to handle bulk data or large data packets.
>
> On the receive side there are at least three problems in the design of a network interface. The first problem is to identify where to store arriving data. The second major problem revolves around the efficient use of empty buffers presented to the network interface by the host. Typically, the receive side has no idea of the frame size until after receiving the entire frame. This poses the problem of finding an appropriate sized empty buffer space at the host. Typical practice is to procure a large empty buffer for every arriving frame."

This apparently has nothing to do with, "a memory said descriptor table for storing a plurality of descriptors for access."

Also, exception is taken with office communication statement above "*by the first and second data processing systems- and descriptor logic for generating [e.g., col. 19, lines 46-47] the descriptors for storage In the descriptor table."* Osborne *col. 19, lines 46-47*, refers to Fig. 9. Osborne "FIG. 9 is a diagrammatic illustration showing dynamic chaining" Osborne *col. 19, lines 46-47* reads:

> "FIG. 9 shows the situation just after the driver/application has enqueued such a frame descriptor in the TXin queue 160."

This apparently has nothing to do with, "*first and second data processing systems- and descriptor logic for generating [e.g., col. 19, lines 46-47] the descriptors for storage in the descriptor table.*" The cited art to Osborne apparently has little or no relevance to claim 1. Thus claim 1 and all claims that depend thereupon are allowable over the cited art.

> *6. As for claim 2, Osborne et al teach the descriptors generated by the descriptor logic comprising a frame descriptor defining a data packet to be communicated between a location in the memory and the second data processing system, and a pointer descriptor identifying the location in the memory [col. 5, lines 53-64].*

In response, the applicants respectfully state that exception is taken with the alleged equivalencies of the elements of claim 2 and Osborne. Claim 2 reads as follows:

2. (original) An apparatus as claimed in claim 1, wherein the descriptors generated by the descriptor logic comprise a frame descriptor defining a data packet to be communicated between a location in the memory and the second data processing system, and a pointer descriptor identifying the location in the memory.

Also, exception is taken with office communication statement above:

"Osborne et al teach the descriptors generated by the descriptor logic comprising a frame descriptor defining a data packet to be communicated between a location in the memory and the second data processing system, and a pointer descriptor identifying the location in the memory [col. 5, lines 53-64]"

Osborne *[col. 5, lines 53-64] reads:*

"More specifically, in order to implement a network interface, either for use in direct access architectures or otherwise, in the subject invention means are provided to identify frames to send to the network interface by utilizing a linked list buffer format in which the ring queues contain multiword frame descriptors. Each such descriptor contains either a pointer to a data buffer, a pointer to the head of a linked list of buffers, or a combination of the two. The remaining words in the frame descriptor contain other information describing the frame, such as the virtual channel number, some state information and various mode indications. Thus in essence, the multiword frame descriptor constitutes a so-called "fat" pointer to the frame data. The normal mode is the so-called Mode M, in which a frame consists of a linked list of buffers. Each buffer in this linked"

Thus, the cited portion of Osborne apparently fails *to* teach "the descriptors generated by the descriptor logic comprising a frame descriptor defining a data packet to be communicated between a location in the memory and the second data processing system." *Thus claim 2 is allowable for itself and because it depends on allowable claim 1.*

7. As for claim 3, Osborne at al teach the descriptor table is stored in the memory of the first data processing system [col. 14, lines 32-35].

In response, the applicants respectfully state that exception is taken with the alleged equivalencies of the elements of claim 3 and Osborne. Claim 3 reads as follows:

3. An apparatus as claimed in claim 1, wherein the descriptor table is stored in the memory of the first data processing system;

The cited portion of Osborne [col. 14, lines 33-35] reads:

"Though the ring queue containing frame descriptors and the buffer descriptors are commonly in host memory, they may also be in network interface local memory."

Osborne apparently fails *to* teach "the descriptor table is stored in the memory of the first data processing system," *or any processing system. Thus claim 3 is allowable for itself and because it depends on allowable claim 1.*

8. As for claim 4, Osborne at SI teach the descriptor table is stored in the memory of the second data processing system [col. 14, lines 32-35].

In response, the applicants respectfully state that exception is taken with the alleged equivalencies of the elements of claim 4 and Osborne. Claim 4 reads as follows:

> 4. An apparatus as claimed in claim 1, wherein the descriptor table is stored in a memory of the second data processing system.

The cited portion of Osborne reads:

> "Though the ring queue containing frame descriptors and the buffer descriptors are commonly in host memory, they may also be in network interface local memory."

Osborne apparently fails *to* teach "the descriptor table is stored in a memory of the second data processing system," *or any processing system. Thus claim 4 is allowable for itself and because it depends on allowable claim 1.*

9. As for claim 5, Osborne et al teach the descriptor table comprising a plurality of descriptors lists sequentially linked together via branch descriptors therein [e.g., figs. 2A- 2C].

In response, the applicants respectfully state that exception is taken with the alleged equivalencies of the elements of claim 5 and Osborne. Claim 5 reads as follows:

> 5. An apparatus as claimed in claim 1, wherein the descriptor table comprises a plurality of descriptor lists sequentially linked together via branch descriptors therein.

The cited portion of Osborne Figs 2A-2C apparently fails to teach a "descriptor table comprises a plurality of descriptor lists sequentially linked together via branch descriptors therein." Thus claim 5 is allowable for itself and because it depends on allowable claim 1.

10. As for claim 6, Osborne et al teach the descriptor table comprising a cyclic descriptor list [col. 1, lines 61-64].

In response, the applicants respectfully state that exception is taken with the alleged equivalencies of the elements of claim 6 and Osborne. Claim 6 reads as follows:

> 6. An apparatus as claimed in claim 1, wherein the descriptor table comprises a cyclic descriptor list.

The cited portion of Osborne reads

> A ring queue, or circular queue, is a common data structure in which a first-in first-out or FIFO queue wraps around, such that the queue occupies a fixed size and extent of memory.

Osborne apparently fails *to* teach a "descriptor table comprises a cyclic descriptor list." *Thus claim 6 is allowable for itself and because it depends on allowable claim 1.*

> *11. As for claim 7, Osborne et al teach the first data processing system comprising a host computer system [fig. 3A).*

In response, the applicants respectfully state that exception is taken with the alleged equivalencies of the elements of claim 7 and Osborne. Claim 7 reads as follows:

> 7. An apparatus as claimed in claim 1, wherein the first data processing system comprises a host computer system.

The cited portion of Osborne Fig 3A apparently fails to teach a " first data processing system comprises a host computer system." Fig 3A is described as:

> FIG. 3A is a block diagram showing an ATM network interface chip on a network interface card in which the subjects frame descriptors and buffer descriptors are used.

Osborne col. 14, lines 21-35 describes Fig. 3A as the following:

> Referring to FIG. 3A, in the subject invention the flexible format of frame descriptors and buffer descriptors permit the aforementioned functions and advantages. To illustrate how this is possible in general, an ATM network interface includes a network interface card 150 and a host computer 151. The frame descriptors and buffer descriptors are used for communication between host 151 and network interface card 150 over peripheral component interconnect or PCI bus 152. The communication includes control information for the ring queues and information describing the data to be transmitted or describing data received. This information belongs to the network interface. Though the ring queue containing frame descriptors and the buffer descriptors are commonly in host memory, they may also be in network interface local memory.

Thus Fig. 3A is not relevant to flow control between data processing systems. Thus claim 7 is allowable for itself and because it depends on allowable claim 1.

12. As for claim 8, Osborne et al teach the second date processing system comprising a data communications interface for communicating data between a host computer system and a data communications network [fig. 3A].

In response, the applicants respectfully state that exception is taken with the alleged equivalencies of the elements of claim 8 and Osborne. Claim 8 reads as follows:

8. An apparatus as claimed in claim 1, wherein the second data processing system comprises a data communications interface for communicating data between a host computer system and a data communications network.

The cited portion of Osborne Fig 3A apparently fails to teach a "second data processing system comprises a data communications interface for communicating data between a host computer system and a data communications network." Fig 3A is described as:

> FIG. 3A is a block diagram showing an ATM network interface chip on a network interface card in which the subjects frame descriptors and buffer descriptors are used.

Osborne col. 14, lines 21-35 describes Fig. 3A as the following:

> Referring to FIG. 3A, in the subject invention the flexible format of frame descriptors and buffer descriptors permit the aforementioned functions and advantages. To illustrate how this is possible in general, an ATM network interface includes a network interface card 150 and a host computer 151. The frame descriptors and buffer descriptors are used for communication between host 151 and network interface card 150 over peripheral component interconnect or PCI bus 152. The communication includes control information for the ring queues and information describing the data to be transmitted or describing data received. This information belongs to the network interface. Though the ring queue containing frame descriptors and the buffer descriptors are commonly in host memory, they may also be in network interface local memory.

Thus Fig. 3A is not relevant to flow control between data processing systems. Thus claim 8 is allowable for itself and because it depends on allowable claim 1.

13. As for clam 9, Osborne et al teach a host computer system having a memory, a data communications interface for communicating data between the host computer system and a data communications network for controlling flow of data between the memory of the host computer system and the data communications interface [fig. 3A].

In response, the applicants respectfully state that exception is taken with the alleged equivalencies of the elements of claim 9 and Osborne. Claim 9 reads as follows:

> 9. A data processing system comprising: a host processing system having a memory, a data communications interface for communicating data between the host computer system and a data communications network, and apparatus as claimed in claim 1, for controlling flow of data between the memory of the host computer system and the data communications interface.

The cited portion of Osborne Fig 3A apparently fails to teach a "a host processing system having a memory, a data communications interface for communicating data between the host computer system and a data communications network, and apparatus ... ... for controlling flow of data between the memory of the host computer system and the data communications interface." Fig 3A is described as:

> FIG. 3A is a block diagram showing an ATM network interface chip on a network interface card in which the subjects frame descriptors and buffer descriptors are used.

Osborne col. 14, lines 21-35 describes Fig. 3A as the following:

> Referring to FIG. 3A, in the subject invention the flexible format of frame descriptors and buffer descriptors permit the aforementioned functions and advantages. To illustrate how this is possible in general, an ATM network interface includes a network interface card 150 and a host computer 151. The frame descriptors and buffer descriptors are used for communication between host 151 and network interface card 150 over peripheral component interconnect or PCI bus 152. The communication includes control information for the ring queues and information describing the data to be transmitted or describing data received. This information belongs to the network interface. Though the ring queue containing frame descriptors and the buffer descriptors are commonly in host memory, they may also be in network interface local memory.

Thus Fig. 3A is not relevant to flow control between data processing systems, etc. Thus claim 9 is allowable for itself and because it depends on allowable claim 1.

> *14. As for claim 10, Osborne et al teach a method comprising controlling flow of data between first and second data processing systems via a memory the steps of controlling comprising: storing [e.g., figs. 2A-2C] in a descriptor table a plurality of descriptors for access [col. 3, lines 2842] by the first and second data processing systems, and by descriptor logic, generating [e.g., col. 19, lines 46-47] the descriptors for storage in the descriptor table, the descriptors including a branch descriptor comprising a ink [e.g., fig. 2A] to another descriptor in the table.*

In response, the applicants respectfully state that exceptions are taken with the alleged equivalencies of the elements of claim 10 and Osborne. Claim 10 reads as follows:

> 10. A method comprising controlling flow of data between first and second data processing systems via a memory, the step of controlling comprising: storing in a descriptor table a plurality of descriptors for access by the first and second data processing systems; and by descriptor logic, generating the descriptors for storage in the descriptor table, the descriptors including a branch descriptor comprising a link to another descriptor in the table.

The cited portion of Osborne apparently fails to teach a "method comprising controlling flow of data between first and second data processing systems via a memory," having a step of controlling." Thus claim 10 is allowable over Osborne.

15. As for claims 11-20, Osborne et al teach the claimed limitations as discussed above.

In response, the applicants respectfully state that indeed the exceptions taken for the apparatus claims are similarly applicable to the method claims. Thus claims 11-20 are allowable each for itself and because each depends on an allowable claim.

Response to Arguments

16. Applicant's arguments see page 10, lines 30-31, filed 4/27/2006, with respect to claims 1-20 have been fully considered and are persuasive. The rejection of claims 1-20 has been withdrawn.

In response, the applicants respectfully express their appreciation for the withdrawal of the rejections.

Claim 21 added to protect a detailed embodiment of the present invention. It is noted that a new and novel combination of even known elements is allowable. It is anticipated that this amendment brings claims 1-21 to allowance. If any questions remain, please contact the undersigned representative before issuing a FINAL action.

Please charge any fee necessary to enter this paper to deposit account 50-0510.

Respectfully submitted,

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